IN THE SPECIFICATION

Please correct the paragraph beginning at page 11, line 22, as follows:

The Gilbert Cell 801 has a first differential pair of transistors Q11 and Q12 and a second differential pair of transistors Q10 and Q9. Emitters of the first differential pair of transistors Q11 and Q12 are directly coupled and connected to a collector of a transistor Q13 forming a current source and a ~~connecter~~ collector of the transistor Q1 of the aforementioned LNA 70. Emitters of the ~~first~~ second differential pair of transistors Q10 and Q9 are directly coupled and connected to a collector of a transistor Q14 forming a current source and a connector of the transistor Q2 of the aforementioned LNA 70. Bases of the first differential pair of transistors ~~Q11~~ Q9 and Q12 are connected to a terminal P11 through a resistor R13, and this terminal P11 is connected to the terminal B1 of the control section 66. Bases of the second differential pair of transistors Q10 and ~~Q9~~ Q11 are connected to the terminal P11 through a resistor R12. Bases of the transistors Q10 and Q11 are connected to a terminal P7 through a capacitor C8, and bases of the transistors Q9 and Q12 are connected to a terminal P8 through a capacitor C7. A local transmission signal (I-ch Local IN) of the I channel is input to the terminals P7 and P8. In addition, collectors of the transistors Q10 and Q12 are connected to the power voltage Vcc through a resistor R1 and a capacitor ~~C13~~ C14 connected in parallel. Collectors of the transistors Q9 and Q11 are connected to the power voltage Vcc through a resistor R2 and a capacitor C13 connected in parallel. The collectors of the transistors Q10 and Q12 are connected to a terminal P13, from which an IOUT+ signal is output. The collectors of the transistors Q9 and Q11 are connected to a terminal P14, from which an IOUT- signal is output.

Please correct the paragraph beginning at page 12, line 23, as follows:

Similarly, the Gilbert Cell 802 has a third differential pair of transistors Q7 and Q8 and a fourth differential pair of transistors Q6 and Q5. Emitters of the third differential pair of transistors Q7 and Q8 are directly coupled and connected to a collector of a transistor Q15 forming a current source and the collector of the transistor Q1 of the aforementioned LNA 70. Emitters of the fourth differential pair of transistors Q6 and Q5 are directly coupled and connected to a collector of a transistor Q16 forming a current source and the collector of the transistor Q2 of the aforementioned LNA 70. Bases of the third differential pair of transistors Q7 and ~~Q8~~ Q6 are connected to the terminal P11 through the resistor ~~R13~~ R10, and this terminal ~~P11~~ P12 is connected to the terminal B1 of the control section 66. Bases of the fourth differential pair of transistors ~~Q6~~ Q8 and Q5 are connected to a terminal P12 through a resistor R11. The bases of the transistors Q6 and Q7 are connected to a terminal P10 through a capacitor C9, and the bases of the transistors Q5 and Q8 are connected to a terminal P9 through a capacitor C10. A local transmission signal (Q-ch Local IN) for the Q channel is input to the terminals P10 and P9. In addition, collectors of the transistors Q6 and Q8 are connected to the power voltage Vcc through a resistor R9 and a capacitor C11 connected in parallel. Collectors of the transistors Q5 and Q7 are connected to the power voltage Vcc through a resistor R3 and a capacitor C12 connected in parallel. The collectors of the transistors Q6 and Q8 are connected to a terminal P15, from which a QOUT+ signal is output. The collectors of the transistors Q5 and Q7 are connected to a terminal P16, from which a QOUT- signal is output.